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EXAMINER	
DINH, NGOC V	
ART UNIT	**PAPER NUMBER**
2187	10

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/963,334	PEREIRA, JOSE P.
	Examiner	Art Unit
	NGOC V DINH	2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-87* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11, 13, 15, 17-42, 45-85, 87* is/are rejected.

7)☒ Claim(s) *12,14,43,44 and 86* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to Amendment filed 12/17/2003.

Claims 15, 17, 30, 43, 48, 52, 61 have been amended.

Claim 16 has been canceled.

Claims 70-87 have been added.

2. Applicant's previous arguments are moot with regard to claims 1-87 in view of the new rejection.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-11, 13, 15-42, 45-85, 87 are rejected under 35 U.S.C.102 (e) as being anticipated by Stark PN 6,633,953.

3. **As per claim 1:**

Stark teaches a content addressable memory (CAM) device comprising:
a first plurality of storage circuits to store an upper value [e.g., upper boundary]; a second plurality of storage circuit to store a lower value [e.g., lower boundary]; and a plurality of compare circuits to determine if a first comparand value is within a range of values defined by the upper value and the lower value [abstract; col. 5, lines 45-60; col. 7, lines 35-65; col. 8, 35-50; col. 27, line 58 to col. 28, line 15].

4. **As per claims 2-4:**

Stark further teaches the first comparand value is a field of bits within a second comparand value [e.g., overlapping range; fig. 10; col. 14, lines 5-20]; each of the first plurality of storage circuits includes a memory element, to store at least one bit

of the upper value [fig. 5; col. 20, lines 35-50]; wherein each of the plurality of compare circuits [e.g., set of comparators; col. 10, lines 13-14] includes circuitry to compare, a bit of the first comparand and to a bit of the upper value and to output a result signal in a first state [e.g., match] if the bit of the: first comparand is greater than the bit of the upper value and to output the result signal in a second state [e.g., mismatch] if the bit of the first comparand is less than the bit of the upper value [col. 9, lines 10-30; col. 10, lines 1-65; col. 20, lines 35-50; the entire claimed section col. 27 to col. 32].

As per claim 5:

Stark further teaches outputting the result signal in a first state comprises switchably coupling a match signal line to a predetermined voltage reference [e.g., logic voltage reference "0" or "1"] to affect a voltage level of the match signal [col. 5, lines 15-35; col. 5, line 63 to col. 6, line 5].

5. As per claim 6:

Inherently Stark teaches outputting the result signal in the second state comprises decoupling the match signal line from the predetermined voltage reference, and coupling the match signal line to a ground voltage reference to pull down the voltage level of the match signal line. This is because in order to toggle the match signal between different logic state, from a first state ["0" or low logic state] to a second state ["1" or high logic state], the match signal first must be discharged to a low logic level [e.g., ground potential] before it is brought high logic level. The only way to discharge the match signal is to decouple it from the predetermined voltage reference and drain the charge [coupling] into ground voltage level.

6. As per claim 7:

Inherently Stark teaches coupling the match signal line to a predetermined voltage reference comprises coupling the match signal line to a ground voltage reference to pull down the voltage level of the match signal line. This is because in order to pull down the match line from logic "1" or high to logic "0" or low, the match line has to be coupled to a ground potential level.

7. As per claims 8-11, 13:

Stark teaches a match line, and wherein a most significant compare circuit of the plurality of compare circuits is coupled to the match line, the most significant compare circuit being adapted to affect a logical state of the match line according to the result signal [col. 10, lines 1-30]; the most significant compare circuit is coupled to output the result signal to the match line; at least one other of the plurality of compare circuits is coupled to output the result signal to the most significant compare circuit [col. 20, line 65 to col. 21 line 10; fig. 2]; the upper and lower value comprises a plurality of bits ordered from a most significant bit to a least significant bit [e.g., least significant q-1], and wherein each of the plurality of compare circuits is adapted to store a respective one of the plurality of bits and to compare the one of the plurality of bits to a respective bit within the first comparand value [col. 13, lines 35-45; col. 23, lines 60-65; col. 24, lines 45-58; col. 25, lines 35-45].

8. As per claims 15:

Stark teaches a content addressable memory (CAM) cell comprising: a first storage circuit to store a first boundary value; a first compare circuit to compare a comparand value to a the first boundary value [fig. 2, 6, 7; col. 28, lines 1-15], the first compare circuit including circuitry to output a first result signal in a first state if the comparand value is greater than the first boundary value and in a second state if the comparand value is less than the first boundary value; and an input to receive a second result signal from another CAM cell, and wherein the circuitry to output the first result signal in the first state is adapted to output the first result signal in the first state [col. 9, lines 10-35; col. 16, lines 59-65; col. 17, lines 5-40; col. 20, lines 35-50; col. 28, lines 1-18].

9. As per claims 17-18:

Stark teaches the circuitry to output the first result signal is further adapted to output the first result signal in the second state [e.g., mismatch] if the comparand value is equal to the first boundary value and the second result signal is in the second state; a second storage circuit to store a second boundary value; and a second compare circuit to compare the comparand value to the second boundary value, the second compare

circuit including circuitry to output a second result signal in the first state [e.g., match] if the comparand is less than the second boundary value and in the second state if the comparand is greater than the second boundary value [col. 9, lines 10-35; col. 16, lines 59-65; col. 17, lines 5-40; col. 20, lines 35-50; col. 28, lines 1-18].

10. As per claim 19:

Stark teaches the circuitry to output the second result signal in the first state is further adapted to output the second result signal in the first state [e.g., match] if the comparand value is equal to the second boundary value [col. 9, lines 20-35]. Inherently, Stark teaches The CAM cell comprising an input to receive a third result signal from a less significant CAM cell and the third result signal is in the first state [e.g., match]. This is because the CAM basically comprises a plurality sets of CAM cells (from most significant CAM cells to less significant CAM cells), each set of CAM cells including memory elements to store a class value that corresponds to one of the plurality of CAM blocks and compare circuitry to compare the stored class value to the class code and to output a respective one of the plurality of select signals in either a first state or a second state according to whether the class code matches the stored class value. In a CAM device, a plurality of CAM cells are cascaded (i.e., coupled serially) such that the output of each serves as an input for the next to CAM devices, and more specifically, to the design and use of a CAM circuit having a plurality of cascaded sub-entries, each sub-entry having a Match-enabled output adapted to enable the CAM search operation of the next sub-entry.

11. As per claims 20-21:

Stark teaches the circuitry to output the first result signal is adapted to output the first result signal in the first state [e.g., TRUE, match] if the comparand is equal to the first boundary value; the circuitry to output the first result signal is adapted to output the first result signal in the second state [FALSE, mismatch] if the comparand is equal to the first boundary value [col. 7, lines 49-53; col. 9, lines 25-35].

12. As per claim 22:

Stark teaches The CAM cell, wherein the first boundary value is an -upper boundary value [col. 4, lines 36-45].

13. As per claim 23:

Stark teaches a content addressable memory (CAM) device comprising:

a first storage circuit to store a first value; and a compare circuit coupled to the first storage circuit to receive the first value and coupled to a mode signal line to receive a mode signal [fig. 6-7], the compare circuit being adapted to compare a comparand value to the first value and to output a first result signal, the first result signal indicating whether the comparand value is greater than the first value when the mode signal is in a first state, and the first result signal indicating whether the comparand is equal to the first value when the mode signal is in a second state [col. 5, lines 45-60; col. 9, lines 10-40].

14. As per claims 24-28:

Starks teaches a second storage circuit to store a second value and coupled to provide the second value to the compare circuit, the compare circuit including circuitry to compare the comparand value to the second value and, when the mode signal is in the first state, to output a second result signal indicating whether the comparand is less than the second value [col. 8, lines 35-45; col. col. 9, lines 15-25];

and a mask circuit coupled to receive the second value from the storage circuit and coupled to the compare circuit, the mask circuit being adapted to selectively mask the first result signal, according to the second value, when the mode signal is in the second state; the mask circuit is adapted to mask the first result signal by preventing [e.g., ignoring "0" value bits] the compare circuit from outputting the first result signal in a state indicative of inequality between the first value and the comparand; the mask circuit is adapted to mask the first result signal by disabling the first value from being received in the compare circuit; the mask circuit is adapted to mask the first result signal by disabling the comparand value from being received in the compare circuit [col. 2, lines 5-17; col. 25, lines 35-65].

15. As per claim 29:

Stark teaches a content addressable memory (CAM) device comprising:

a first storage circuit to store a first value; and a first compare circuit coupled to receive the first value from the first storage circuit and having a select input to receive

a level select signal, the first compare circuit being adapted to compare a comparand value to the first value and to assert a beyond boundary signal if the level select signal is in a first state and if the comparand value is greater than the first value, the first compare circuit being further adapted to assert the beyond boundary signal if the level select signal is in a second state and if the comparand value is less than the first value [col. 9, lines 8-40; col. 10, lines 1-40; col. 21, lines 25-55; col. 28, lines 1-20].

16. As per claims 30-32:

Stark teaches the CAM device further comprising:

A first input to receive a first signal representative of the comparand value; a second input to receive a second signal representative of a complement of the comparand value; and a select circuit [701, fig. 7] coupled to the first input and the second input to select according to a state of the level select signal, either the first signal or the second signal to be output to the compare circuit for comparison with the first value [col. 10, lines 1-30];

the CAM device, wherein the select circuit is a multiplexer [901, fig. 9] having a control input coupled to receive the level select signal and having first and second ports coupled respectively to the first and second inputs; the CAM device, wherein the first value is representative of an upper boundary value when the level select signal is in the first state, and wherein the first value is representative of a lower boundary value when the level select signal is in the second state [fig. 9; col. 4, lines 36-65; col. col. 20, lines 35-55].

17. As per claims 33-34:

Stark teaches the CAM device further comprising a mode select input [802, 806, fig. 8-9] to receive a mode select signal, the first compare circuit being enabled to assert [e.g., TRUE, match] the beyond-boundary signal if the mode select signal is in a first state and the first compare circuit being disabled [FALSE, mismatch, masking bits] from asserting the beyond boundary signal if the mode select signal is in a second state [col. 12, lines 23-55; col. 20, lines 42-52];

the CAM device further comprising a second compare circuit to compare the comparand value and the first value and to assert a match signal indicative of whether

the comparand value is equal to the first value, the second compare circuit being enabled to assert the match signal if the mode select signal is in the second state, and the second compare circuit being disabled from asserting the match signal if the mode select signal is in the first state [col. col. 9, lines 10-35; col. 20, lines 35-50].

18. As per claim 35:

Stark teaches a content addressable memory (CAM) device comprising:

a CAM array having a plurality of CAM cells; and at least one mode select line coupled to at least one set of CAM cells within the plurality of CAM cells [fig. 8], the set of CAM cells being adapted to compare a comparand value to a range defined by at least one boundary value stored within the set of CAM cells if a mode select signal on the mode select line is in a first state [e.g., match/ TRUE, "1"], and the set of CAM cells being adapted to compare the comparand value for equality with a data value stored within the set of CAM cells if the mode select signal is in a second state [e.g., mismatch, FALSE, "0"; "an ordered set of storage device containing boundary type bits each of which corresponds to a memory cell in the Entry List storage device, and is utilized for storing **"1"** whenever a **closed boundary** is stored in the corresponding memory cell, and for storing **"0"** whenever an **opened boundary** is stored in the memory cell"; col. 10, lines 52-57; col. 4, lines 1-20; col. 5, lines45-60].

19. As per claim 36-39:

Stark teaches the CAM device further comprising: a mode configuration circuit [701, fig. 7] coupled to the mode select line, the mode configuration circuit including a storage circuit to store a mode value [e.g., Range mode, Ternary mode, binary mode] the mode select signal being in either the first state or the second state according to the mode value; an interface [data bus 805, fig. 8] to receive a first instruction from a host processor, the CAM device being adapted to store the mode value in the storage circuit in response to the first instruction; a mode select interface [701, fig. 7], and wherein the mode select line is coupled to the mode select interface to receive the mode select signal from an external device, wherein the external device is a host processor [col. 10, lines 39-40; col. 11, lines 19-30; col. 15, lines 47-50; col. 24, lines 15-20; col. 30, lines 45-50].

20. As per claim 40:

Stark teaches a system comprising: a processor and a content addressable memory (CAM) device coupled to receive instructions and data values from the processor, the CAM device including a plurality of CAM cells [fig. 7] and being responsive to a first instruction from the processor to select either a first operating mode [e.g., range mode] or a second operating mode [e.g., ternary mode] for the plurality of CAM cells, the plurality of CAM cells being adapted to compare a comparand value to a range defined by at least one boundary value stored within the plurality of CAM cells if the first operating mode is selected, and the plurality of CAM cells being adapted to compare the comparand value for equality with a data value stored within the plurality of CAM cells if the second operating mode is selected [col. 4, 8-20; col. 9, lines 15-30; col. 12, lines 23-40; col. 15, lines 47-50].

21. As per claims 41-42:

Stark teaches the CAM device includes: a mode configuration circuit to store a mode select value in response to the first instruction, the mode select value indicating the first operating mode [e.g., range mode] or the second operating mode [e.g., ternary mode] according to the first instruction; the plurality of CAM cells is responsive to the mode select value to operate in either the first operating mode or the second operating mode [col. 2, lines 55-65; col. 12, lines 23-40].

22. As per claims 45-47:

Stark teaches a system comprising:

a processor; and a content addressable memory (CAM) device coupled to receive instructions from the processor [fig. 7-8], the CAM device including a first plurality of CAM Cells and being responsive to a first instruction from the processor to store a first boundary value in the first plurality of CAM cells, the first plurality of CAM cells being adapted to compare the first boundary value with a first comparand value in a compare operation and to output a first result signal indicative of whether the first comparand value is greater than the first boundary value [col. 7, lines 45-60; col. 28, lines 1-15];

the first plurality of CAM cells are responsive to a mode select signal to operate in either a range mode or a ternary mode, the first plurality of CAM cells being adapted to output the first result signal when operated in the range mode [col. col. 2, lines 55-65; col. 12, lines 23-40]; the first plurality of CAM cells are responsive to a mode select signal to operate in either a range mode or a binary mode, the first plurality of CAM cells being adapted to output the first result signal when operated in the range mode [col. 24, lines 11-18].

23. As per claim 48:

Stark teaches the CAM device includes a second plurality of CAM cells to store a data value, the second plurality of CAM cells being adapted to compare the data value with a second comparand value in a compare operation and to output a first result signal indicative of whether the second comparand value is equal to the data value [fig. 6; col. 9, lines 25-32].

24. As per claims 49-50:

Stark teaches the first plurality of CAM cells and the second plurality of CAM cells are each included within a first row of CAM cells within the CAM device; the first comparand value and the second comparand value each constitute a respective field of bits within a third comparand value [e.g., cascaded structure; consecutive bits; fig. 8; col. 5, line 63 to col. 6, line 5].

25. As per claims 51-52:

Stark teaches the CAM device is further responsive to the first instruction from the processor to store a second boundary value in the first plurality of CAM cells, and the first plurality of CAM cells being further adapted to compare the second boundary value with the second comparand in the compare operation and to output a second result signal indicative of whether the first comparand value is less than the second boundary value col. 7, lines 44-55; col. 28, lines 1-15];

the CAM device includes multiple independently searchable storage blocks [fig. 8] each including a plurality of CAM cells therein, the first plurality of CAM cells being included within the plurality of CAM cells in one of the searchable storage blocks [fig. 7-8].

26. As per claims 53-54, 56:

Stark teaches the CAM device includes a block configuration circuit to store a block configuration value [701, fig. 7]. Implicitly, Stark teaches a circuitry to configure at least one of the storage blocks to have a storage width and depth according to the block configuration value; wherein the CAM device is responsive to a second instruction from the processor to store the block configuration value/mode value in the block configuration circuit. This is because the CAM comprises a block configuration to store information about the depth and width of CAM device. When the user input a retrieval key word (comparand), the key word storage in the CAM is then searched to determine if the retrieval key word (comparand) is matched/mismatched a key word stored inside the CAM. If the retrieval key word inputted by the user is larger (width, depth) than the size of the current available CAM device, the processor will concatenate/cascade additional CAM devices to form a new larger CAMs device in order to accommodate the size of the new retrieval key word, then the processor will store the new larger CAMs device (width, depth) word back to the block configuration circuit.

27. As per claims 55, 57:

Stark teaches the block configuration is adapted to store a mode value, and wherein the first plurality of CAM cells are responsive to the mode value to operate in either a range mode or a ternary mode/Binary mode [RCAM Range Content Addressable Memory/ TCAM Ternary Content Addressable Memory, col. 12, line 1; col. 15, lines 45-50], the first plurality of CAM cells being adapted to output the first result signal when operated in the range mode [col. 2, lines 55-65; col. 12, lines 23-40].

As per claims 58:

Claim 58 is rejected as the same reasons as set forth in claim 45 due to the same scope.

28. As per claim 59:

Stark teaches storing the first boundary value in the plurality of CAM cells in response to a write instruction [e.g., storing/extracting associated data values; col. 4, lines 8-20].

29. As per claim 60:

Stark teaches comparing the comparand value with the first boundary value comprises, in each CAM cell of the plurality of CAM cells, asserting a greater-than signal if either (1) a bit of the comparand value received within the CAM cell is greater than a bit of the first boundary value stored within the CAM cell, or (2) the bit of the comparand value is equal to the bit of the first boundary value and a greater-than signal is received from a less significant CAM cell [e.g., least significant q-1 line, col. 24, lines 45-50; left most bit, col. 13, lines 35-40] within the plurality of CAM cells [col. 5, lines 45-60].

30. As per claims 61-64:

Stark further teaches: a greater than signal asserted by a most significant one of the plurality of CAM cells constitutes the first result signal [col. 25, lines 35-45]; comparing a comparand value with a second boundary value stored in the plurality of CAM cells; and asserting a second result signal if the comparand value is less than the second boundary value [col. 9, lines 15-30];

comparing the comparand value with the second boundary value comprises, in each CAM cell of the plurality of CAM cells, asserting a less-than signal if either (1) a bit of the comparand value received within the CAM cell is less than a bit of the second boundary value stored within the CAM cell, or (2) the bit of the comparand value is equal to the bit of the second boundary value and a less-than signal is received from a less significant CAM cell within the plurality of CAM cells; a less-than signal asserted by a most significant one of the plurality of CAM cells constitute the second result signal [col. 13, lines 20-50; col. 14, lines 1-30; col. 25, lines 35-50].

31. As per claim 65-69:

Claims 65-69 are the claimed apparatus CAM device corresponding to the claimed method in claims 58, 59, 60, 62 and 63. Therefore claims 65-69 are rejected as the same reason as set forth in claims 58-60, 62-63.

32. As per claims 70-74:

Stark teaches a CAM device comprising: at least one range compare cell configured to store a bit of a range limit, wherein the at least one range compare cell is further

configured to output a result signal that indicates at least whether the stored range limit bit is greater than or less than a corresponding bit of a comparand; and at least one CAM cell configured to store a data bit, wherein the at least one CAM cell is further configured to output a match signal that indicates whether the stored data bit matches a corresponding bit of a comparand, wherein at least one range compare cell and at least one CAM cell are coupled to a common match line [fig. 8; col. 4, lines 8-35; col. col. 5, lines 45-60; col. 9, lines 1-35].

Stark further teaches the CAM device wherein: the at least one CAM cell comprises a ternary CAM cell; the at least one CAM cell comprises a binary CAM cell; the at least one range compare cell comprises a configurable cell that selectively operates in one of a range compare cell mode, and a ternary CAM cell mode [col. 2, lines 55-60]; the at least one range compare comprises a configurable cell that selectively operates in one of a range compare cell mode and a binary CAM cell mode [col. 2, lines 55-65; col. 12, lines 23-40; col. 15, lines 47-50; col. 13, lines 5-20; col. 24, lines 15-20].

33. As per claim 75:

Stark teaches the CAM device wherein the at least one range compare cell comprises: at least one less significant range compare cell configured to output the result signal to a next more significant range compare cell, wherein the result signal is dependent on a result of a comparison of the stored range limit bit and the corresponding comparand bit and a result signal output from a next less significant range compare cell; and a most significant range compare cell configured to output a final result signal to the common match line, wherein the final result signal indicates at least whether the comparand is greater than or less than the stored range limit [e.g., at least one of the extreme values of each associative element is stored in the first storage area in a location that corresponds to the priority of the associative element; and each value of the associated data set is stored in a location in the second storage area, that corresponds to the location of the associative element to which it is associated; col. 3, lines 58-63; compared most significant bits from left to right; col. 25, lines 40-44; col. 23, lines 45-50; col. 28, lines 30-35].

34. As per claims 76-77:

Stark teaches the CAM device wherein the result signal further indicates whether the stored range limit bit is equal to a corresponding comparand bit; wherein the final result signal output to the common match line further indicates whether the stored range limit is equal to the comparand [col. col. 7, lines 45-5].

35. As per claim 78:

Stark teaches a method for performing a range comparison operation in a content addressable memory (CAM) device to determine whether a comparand is within a range, the method comprising: storing at least one range limit in a plurality of range compare cells, including a most significant range compare cell [e.g., upper boundary], and a plurality of less significant range compare cells [e.g., lower boundary] for storing bits of the range limit according to their significance [e.g., the most specific match; col. 2, lines 15-17; closed boundary "1", opened boundary "0"; col. 10, lines 52-57]; comparing bits of the comparand with corresponding bits of the range limit; outputting a result signal for each range compare cell based on the bit comparison, and on a result signal output by a next less significant range compare cell; and outputting a final result signal from the most significant range compare cell to a match line, wherein the final result signal indicates at least whether the comparand is greater than or less than the range limit [fig. 7-8; col. 5, lines 45-55; col. 9, lines 10-30; col. 13, lines 35-45].

36. As per claims 79-84:

Stark teaches:

the at least one range limit includes an upper range limit, and wherein the final result signal indicates the comparand is within the range when the comparand is less than [e.g., closed boundary col. 10, lines 45-50] the upper range limit [fig. 5; T(t-1) <= K<Tt; col. 20, lines 35-40];

the at least one range limit includes a lower range limit, and wherein the final result signal indicates the comparand is within the range when the comparand is greater than [e.g., closed boundary] the lower range limit [fig. 5; T(p+1)<=K, T(p+2); col. 20, lines 42-45];

the at least one range limit includes an upper range limit, and wherein the final result signal indicates the comparand is within the range when the comparand is less than the upper range limit or equal [e.g., opened boundary, col. 10, lines 52-57] to the upper range limit [col. 20, lines 35-65];

the at least one range limit includes a lower range limit, and wherein the final result signal indicates the comparand is within the range when the comparand is greater than or equal to the lower range limit [col. 20, lines 35-65].

37. As per claims 85:

Stark teaches the plurality of range compare cells comprises a plurality of configurable cells [fig. 8], including a most significant configurable cell, and a plurality of less significant configurable cells for storing bits of at least one stored value according to their significance [col. 28, lines 25-40], the method further comprising, setting a mode select signal, to select a range compare mode or a ternary CAM mode [RCAM Range Content Addressable Memory/ TCAM Ternary Content Addressable Memory, col. 12, line 1; col. 15, lines 45-50] wherein, in the ternary CAM mode, the at least one stored value comprises a data word and a mask word, and wherein, in the range compare mode, the at least one stored value comprises an upper range limit and a lower range limit [col. 2, lines 1-15; col. 4, lines 8-20].

38. As per claim 87:

Stark teaches a CAM comprising: a match line [806, fig. 8]; and a plurality of CAM cells including storage circuits to store an upper bound value and a lower bound value and compare circuits fig. 2, 6, 7] coupled to the storage circuits, wherein the plurality of CAM cells are coupled in a chain ordered from a least significant compare circuit to a most significant compare circuit to compare a comparand value with the upper and lower boundary values, and to resolve a compare result from the least significant compare circuit to the most significant compare circuit, and wherein the most significant compare circuit couples the plurality of CAM cells to the match line [col. 10, lines 52-65col. 13, lines 35-40; col. 24, lines 45-50; col. 25, lines 40-50].

Allowable Subject Matter

39. As per claims 12, 14, 43-44, 86

Claims 12, 14, 43-44, 86 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

40. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ngoc Dinh whose telephone number is (703) 305-3023. The examiner can normally be reached on Monday-Friday 8:30 AM-5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks, can be reached on (703) 308-1756. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

NGOC DINH
Patent Examiner
ART UNIT 2187
March 16, 2004

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